REMARKS/ARGUMENTS

This Reply is responsive the Office Action mailed to counsel for the Applicants on July 10, 2003. Claims 1-35 are pending in this Application. In this Reply, Applicants correct the minor informalities noted in claims 20 and 25-35 by way of amendments to claims 20 and 25. No new matter is added by way of this Reply.

Allowable Subject Matter

Applicants note with appreciation the Examiner's indication that claims 11-19 and 21-24 are allowed, and that claims 20 and 25-35 are allowable once minor informalities were corrected. As described below, Applicants have amended claims 20 and 25 to correct the informalities noted by the Examiner.

Information Disclosure Statement

Applicants submitted an IDS on May 21, 2003 but have not received a copy thereof initialed by the Examiner. Applicants request that the Examiner indicate his consideration of the art submitted by the Applicants in the IDS.

Claim Objections

Applicants have amended claims 20 and 25, as well as paragraph [003] of the specification as suggested by the Examiner. Applicants also have amended paragraphs [003] and [004] to correct a typographical error. Prior to the amendments, paragraphs [003] and [004] recited an "AC" coupling but now correctly recite a "resistor-capacitor (RC)" coupling as contained in Fig. 1 of this Application. Accordingly, Applicants believe that the Examiner's objections to claims 20 and 25-35 have been obviated and that the claims are now allowable.

Claim Rejections – 35 U.S.C. § 102

The Examiner has stated that he believes U.S. Pat. No. 4,983,817 to Dolash et al. (Dolash) anticipates claims 1-2 and 4 because Dolash allegedly teaches a background compensating bar code reader that detects a fluorescent light signal 10 serving as the detect signal by receiving light reflected from a target and reflected excitation light signal 11 serving as the signal for generating of the baseline signal. Specifically, the Examiner has stated that he believes the Dolash's alleged detection and conversion of reflected excitation light signal 11 into voltage signal 31 teaches the "generating a baseline signal" step of

Applicants' claim 1, that Dolash's alleged detection and conversion of fluorescent light signal 10 into voltage signal 18 teaches the "generating a detected signal" step of Applicants' claim 1, and that Dolash's alleged subtraction of voltage signal 31 from voltage signal 18 teaches the "subtracting" step of Applicants' claim 1. Applicants respectfully disagree with Examiner.

Dolash fails to teach, disclose, or suggest the baseline generation step of claim 1. Claim 1 explicitly states that the baseline is generated by sampling light reflected from the target and the background, if any, *before* a light scan is transmitted at the target. Dolash on the other hand, explicitly and unambiguously relies on samples of light reflected from the background *as a direct result of transmitting a light scan at the target and background* to generate its so-called baseline signal. This is not a difference without a distinction. Claim 1's generation of the baseline signal before a light scan is transmitted at the target allows one to use the absence of any reflected light from the target (sometimes referred to by those skilled in the art as the "dark zone") as a reference point in the subsequent processing of the progressively corrected scan signal generated in the subtracting step of claim 1. This information is lost, however, when the method taught by Dolash is practiced. Accordingly, Dolash fails to teach or disclose all the elements in Applicants' claim 1 and the rejections under 35 U.S.C. § 102 should be withdrawn.

Claim Rejections – 35 U.S.C. § 103

As noted above, Dolash fails to teach, disclose, or any way suggest the subject in claims 1-2 and 4. Accordingly, given that all of the Examiner's rejections of claims 3 and 5-10 under 35 U.S.C. § 103 rely exclusively on combinations of Dolash with the alleged teachings of other art, whether proper or not, must be withdrawn. Moreover, Applicants respectfully submit that one ordinarily skilled in the art at the time the invention was made would not have looked to, considered, or been motivated to make the combinations utilized by the Examiner. Regarding some of the other art in particular, Applicants note the following.

The examiner has stated that he believes Dolash fails to teach subtracting a baseline signal from a detected signal by inverting the baseline signal and summing the inverted signal with the detected signal, but that U.S. Pat. No. 5,892,745 (Belser) does. The Examiner then concludes that it would have been obvious to one ordinarily skilled in the art to combine the

teachings of Dolash and Belser to achieve Applicants' claim 10. Applicants agree that Dolash, in addition to its other shortcomings, fails to provide the foregoing teaching. However, even if Dolash did provide the other teachings the Examiner has stated in his § 102 rejections, which it does not, Applicants respectfully submit that one ordinarily skilled in the art would be motivated to combine or even consider Belser in solving the problems faced by Applicants. The subject matter in claim 6 uses inversion and summing of the baseline and detected signals to establish a zero (0) volt reference in a signal that may contain an unpredictable offset. Belser teaches no more than the ability to subtract two signals by inverting one and summing it with the other. Belser fails in any way, shape, or form to discuss or suggest ways of solving the problems in the prior art overcome by the Applicants.

The examiner has stated that he believes Dolash fails to teach generating a scan synchronization signal immediately before transmitting the light scan and generating the baseline signal immediately after generating the scan synchronization signal, but that U.S. Pat. No. 4,806,741 (Robertson) teaches "a line scan synchronization signals which comprise steps of generating a time sequence of pulsed signals." The Examiner then concludes that it would have been obvious to one ordinarily skilled in the art to combine the teachings of Dolash and Robertson to achieve Applicants' claim 10. Applicants agree that Dolash, in addition to its other shortcomings, fails to provide the teaching noted above. However, even if Dolash did provide the other teachings the Examiner has stated in his § 102 rejections, which it does not, Applicants respectfully submit that Robertson fails to teach, disclose, or suggest using a scan synchronization signal for timing when to generate the baseline signal; and moreover, that one ordinarily skilled in the art would not have combined or even considered Robertson in attempting to solve the problems overcome by Applicants' claim 10. In typical bar code and other such readers the scan synchronization signal is related to the position of the mechanically rotating mirror that directs the light scan generated by the reader at the target. Robertson provides no such teachings, disclosures, or suggestions.

Conclusion

Applicants respectfully submit that none of the rejections can stand, and that all of the objections to minor informalities have been remedied. Accordingly, all of the claims in this Application are in a condition for immediate allowance.

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David L. Marcus
Registration No. 46,897

Woodcock Washburn LLP
One Liberty Place - 46th Floor
Philadelphia PA 19103
Telephone: (215) 568-3100
Facsimile: (215) 568-3439